UNIVERSITÀ DEL PIEMONTE ORIENTALE

Reliability of multi-core systems-on-chip by interacting Markovian agents

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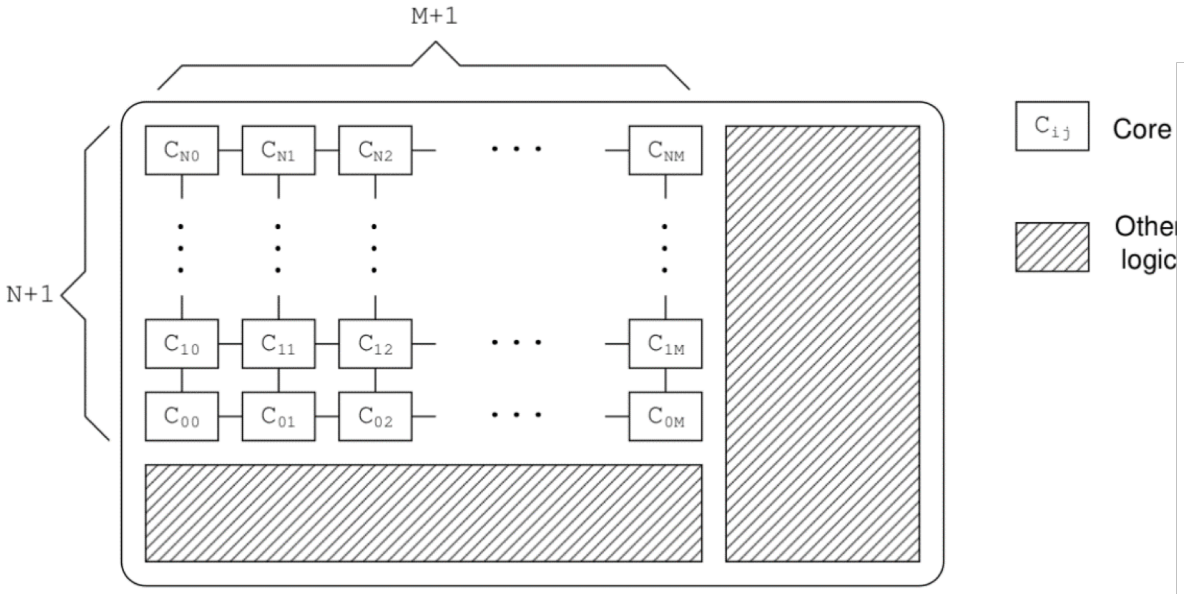
Motivations

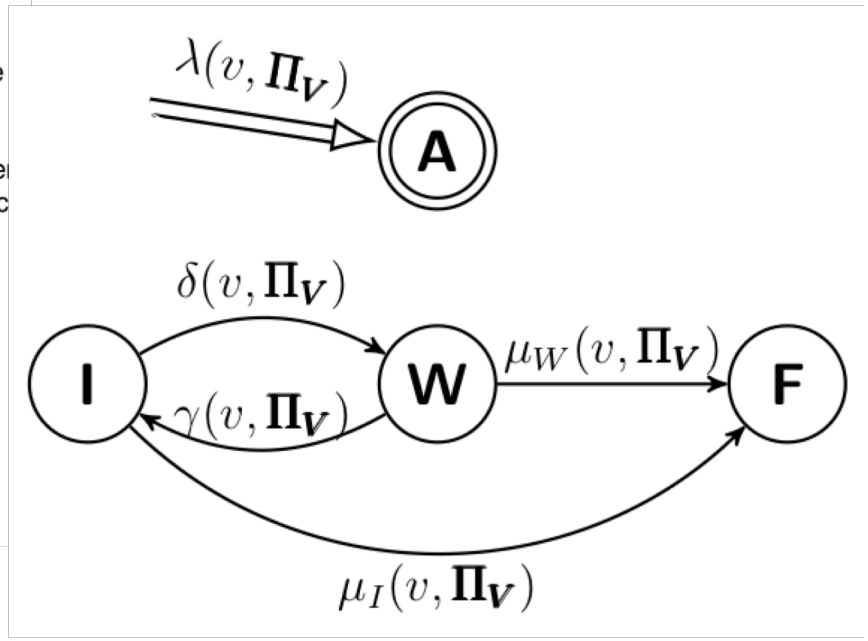
- Advances in chip manufacturing process led to
  - shrink the dimension of transistors to tens of nanometers
  - Increase aging phenomena
- Integration of several components in same chip increases
  - Current densities
  - Operating temperature
- Such effects reduce device reliability and lifetime

Modeling challenges

- The model should handle:
  - Realistic non-Markovian reliability and lifetime distributions
  - Workload variations
  - Interdependencies between:
    - Workload – Temperature
    - Temperature – Reliability
    - Geometry-dependent heat diffusion among cores

Model





$$\begin{cases} \dfrac{d\,\boldsymbol{\pi}_c^D(t;v)}{d\,t} = \boldsymbol{\pi}_c^D(t;v)\,\boldsymbol{K_c}(t;v;[\mathbf{\Pi_V}]) \\ \dfrac{d\,\boldsymbol{\pi}_c^R(t;v)}{d\,t} = \boldsymbol{d}_c(t;v;\mathbf{\Pi_V}) \end{cases}$$

Aging model

- Lifetime reliability of a digital component modeled as a Weibull distribution*

$$R(t,T) = e^{-\left(\frac{t}{\alpha(T)}\right)^{\beta}}$$

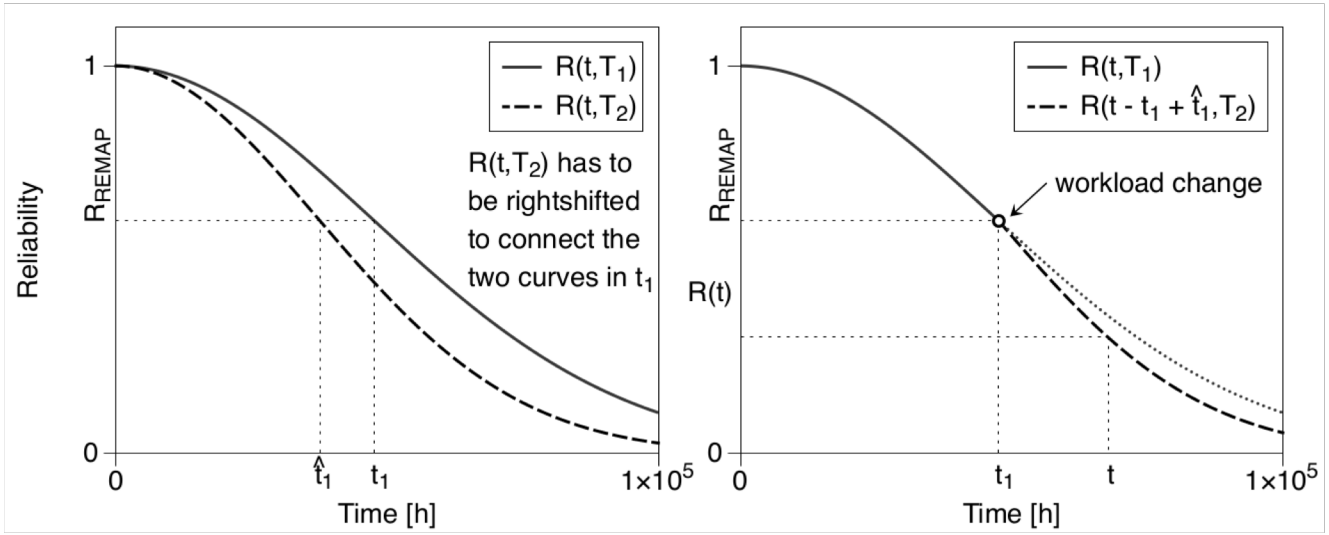
with

$$\alpha(T)_{EM} = \frac{A_0 (J - J_{\text{crit}})^{-n} e^{\frac{E_a}{kT}}}{\Gamma\left(1 + \frac{1}{\beta}\right)}$$

Black equation for electromigration

$$\beta = 2$$

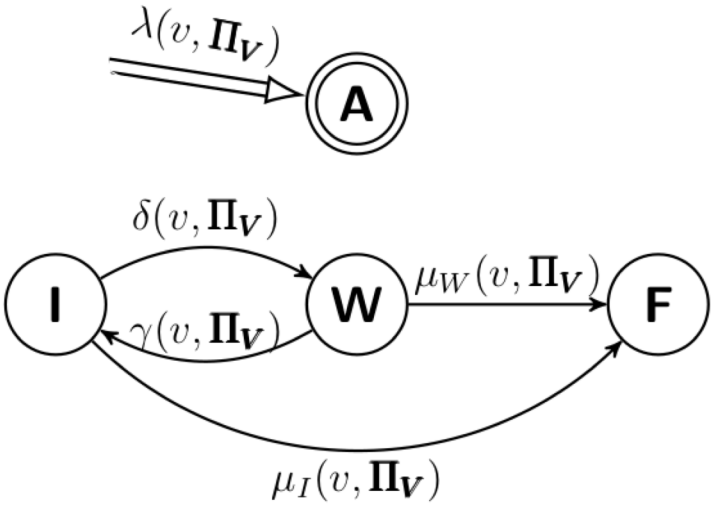
when workload changes also T may vary, but *reliability conserves*, so:



* JEDEC Solid State Tech. Ass. Failure mechanisms and models for semi-conductor devices. JEDEC Publ. JEP122G, 2010

Aging model

$$A = H_Y(t) = \int_0^t h_Y(u)du$$

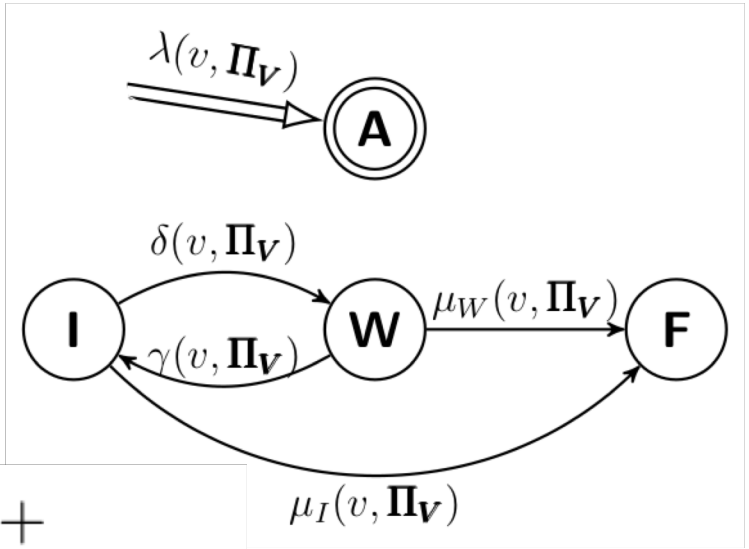


$$f_W(t) = \frac{\beta}{\alpha}\left(\frac{t}{\alpha}\right)^{\beta-1} e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad F_W(t) = 1 - e^{-\left(\frac{t}{\alpha}\right)^{\beta}}$$

$$h_W(t) = \frac{\beta}{\alpha}\left(\frac{t}{\alpha}\right)^{\beta-1} \quad H_W(t) = \left(\frac{t}{\alpha}\right)^{\beta}$$

$$H_W^{-1}(A) = \alpha A^{\frac{1}{\beta}} \quad \lambda_W(A) = \frac{\beta}{\alpha} A^{\frac{\beta-1}{\beta}}$$

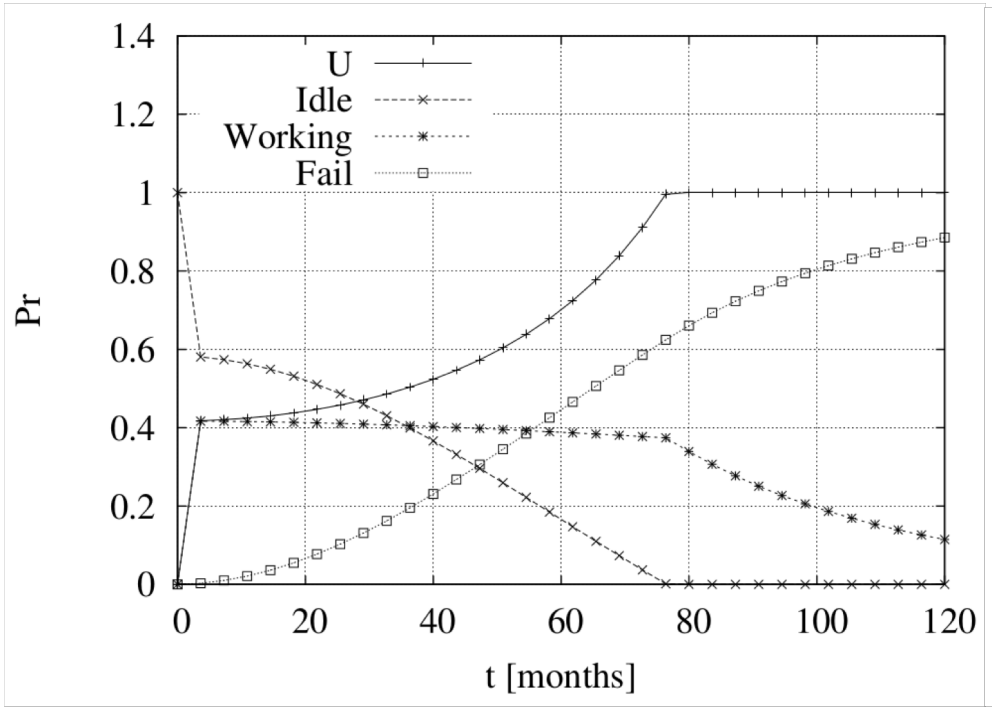
Thermal model

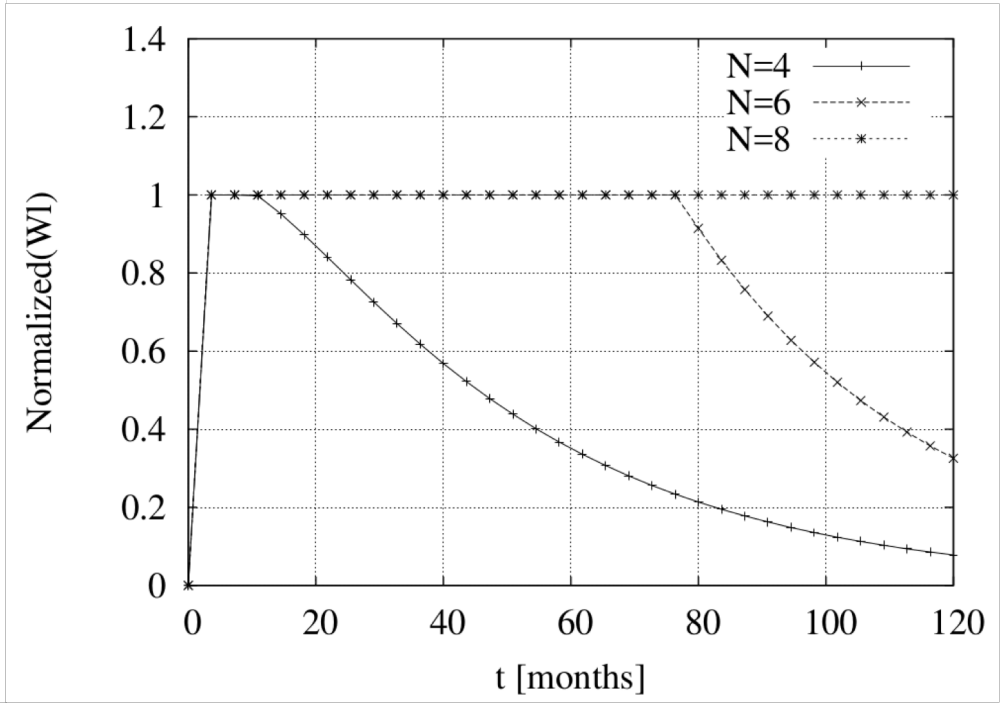


$$
\begin{aligned}
U_S(i,j) &= \pi_W(t; v_{i+1,j}) + \pi_W(t; v_{i-1,j}) + \\
&+ \pi_W(t; v_{i,j+1}) + \pi_W(t; v_{i,j-1}) \\
U_C(i,j) &= \pi_W(t; v_{i+1,j+1}) + \pi_W(t; v_{i+1,j-1}) + \\
&+ \pi_W(t; v_{i-1,j+1}) + \pi_W(t; v_{i-1,j-1})
\end{aligned}
$$

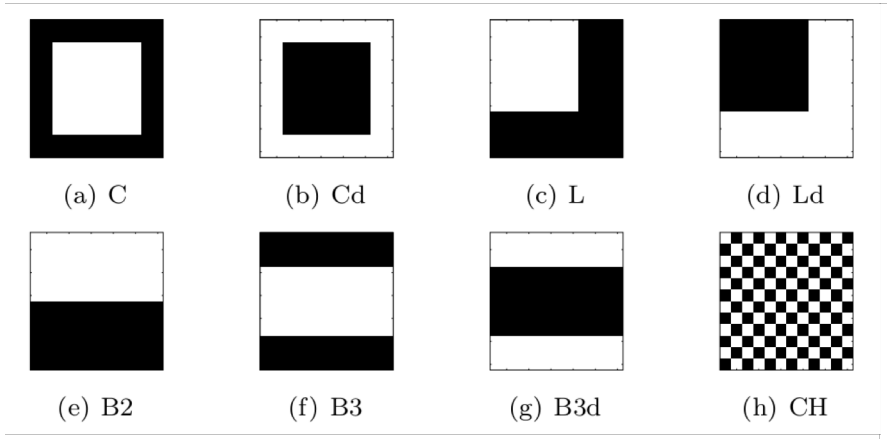
$$
\begin{aligned}
T_W(i,j) &= c_0 + c_2 \cdot U_S(i,j) + c_3 \cdot U_C(i,j) \\
T_I(i,j) &= c_0 + c_1 + c_2 \cdot U_S(i,j) + c_3 \cdot U_C(i,j)
\end{aligned}
$$

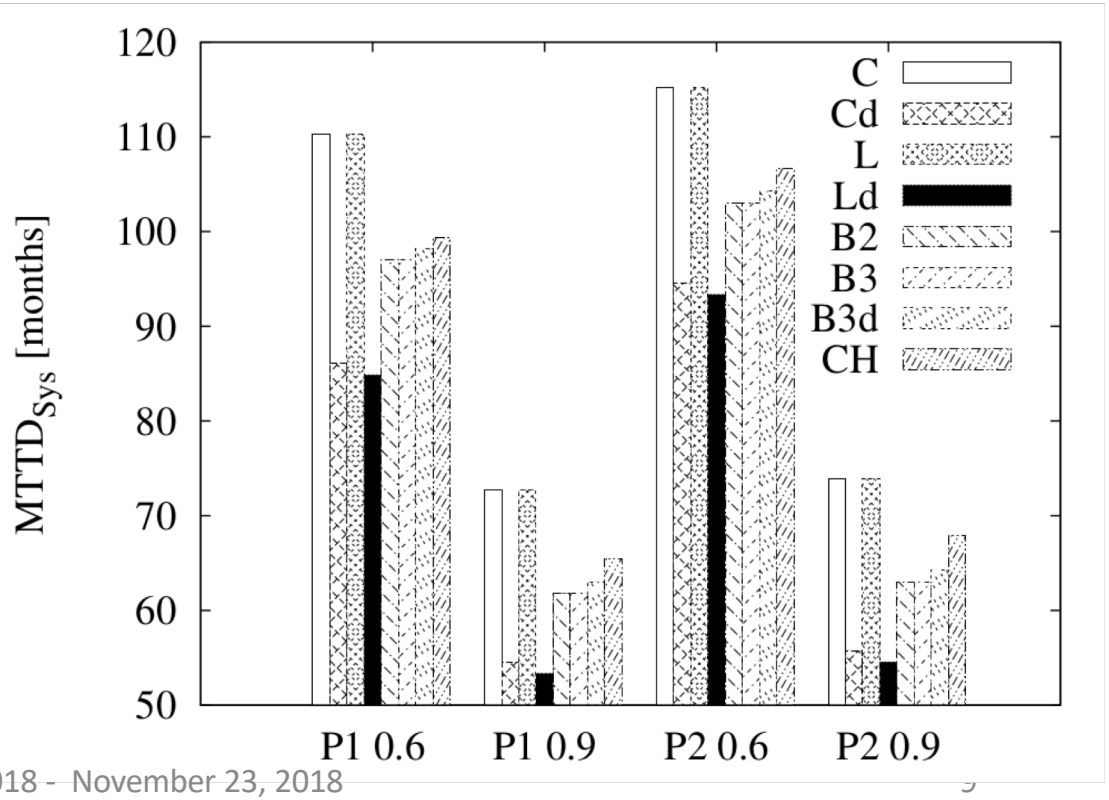
- In the first scenario we assume:
  - uniform workload over a system with 36 cores
  - Per-core utilization 40%

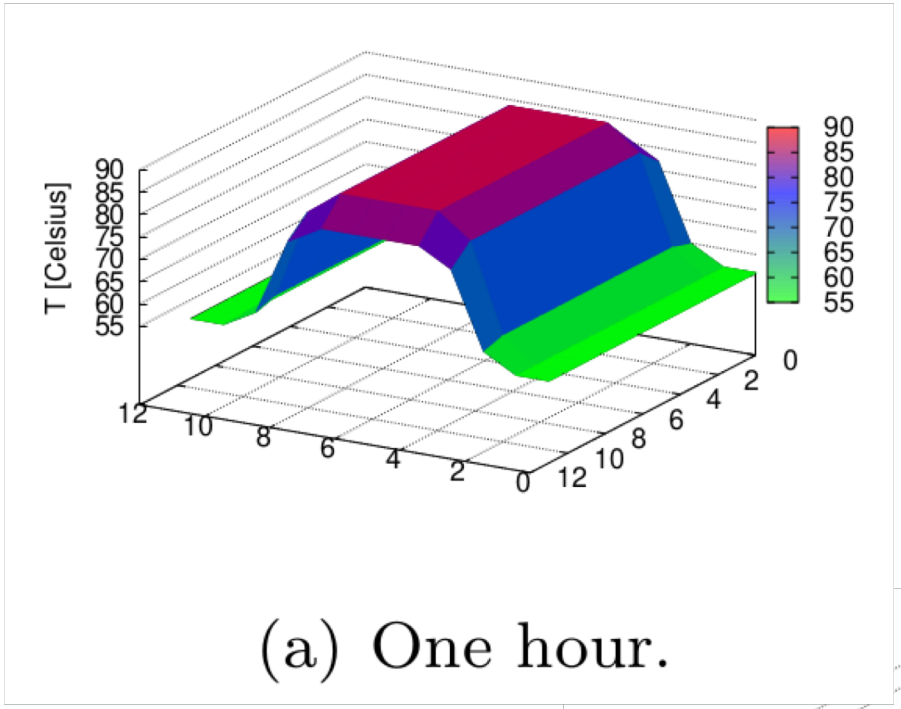




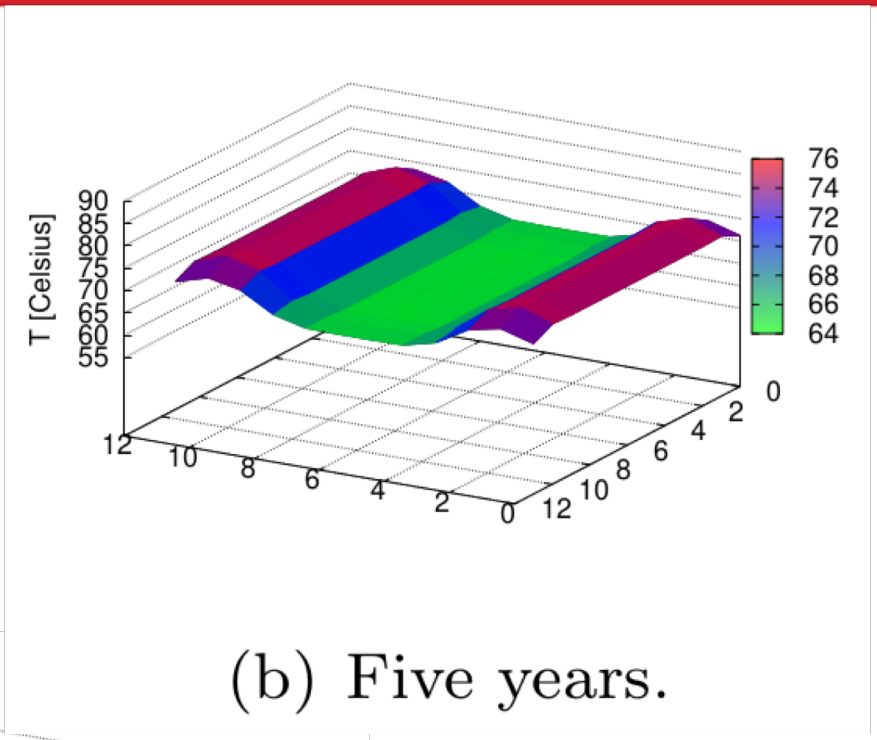
- In the second scenario we assume:
  - A 144 core-CPU with primary and spare core
  - Per-core utilization 60% and 90%



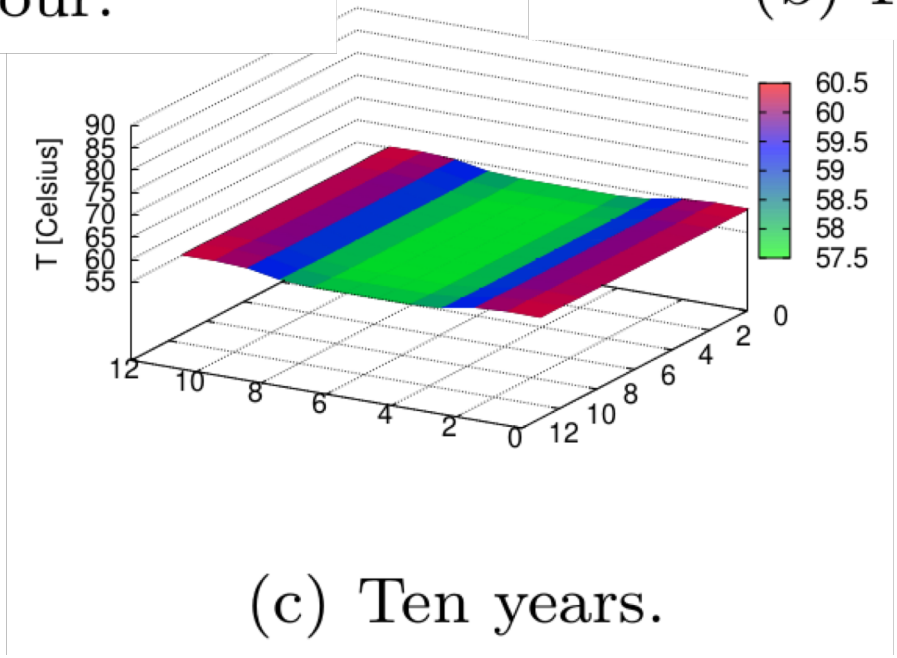




(a) One hour.



(b) Five years.



(c) Ten years.